



# My Vision for the Future

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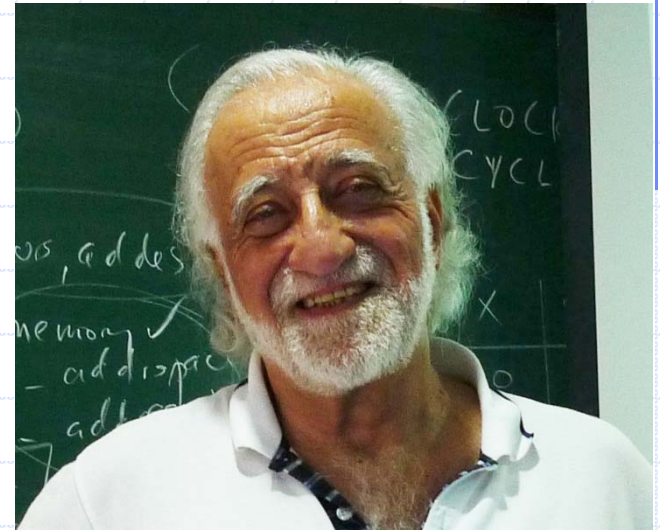
Celebrating Yale@75

University of Texas, Austin

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# General-Purpose Microarchitectures

- ◆ Yale has done it all
- ◆ If Yale has not then Guri has



need to find something else to do!

# Multicores which are easy to program

- ◆ It would be a good problem to work on provided you have some fresh ideas

just remember that every architect believes that his machine is very programmable  
- ask Bill



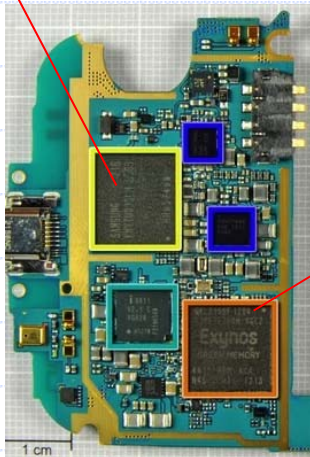
# Power constraints are the real challenge

- ◆ Even though as a community we are very poor at measuring power/energy in architectures, some facts remain
  - Functionality of hand-held devices is determined primarily by power/energy issues
  - There is no better way to reduce power dramatically than to replace compute-intensive software by special purpose hardware

# Cell Phones: Samsung Galaxy S III April 2012

Quad core ARM  
is just one of  
the complex  
blocks

16GB  
NAND flash



Samsung Exynos Quad:

- quad-core A9
- 1GB DDR2 (low power)
- Multimedia processor
- ...

power consumption < 1W

# Design of systems embodying special-purpose hardware



## *Challenges*

- ◆ SW stack has to run on ever changing special purpose HW
- ◆ Exact HW-SW decomposition is often not clear until one is deeply into design
- ◆ Functional verification
- ◆ Power-Performance exploration

# Need a design methodology where

- ◆ Specs are agnostic to HW/SW implementations
- ◆ Blocks can be “composed in parallel” to form bigger blocks
- ◆ Tools for designing blocks can be domain specific
- ◆ Spec and Implementation can continually evolve
- ◆ Modular refinement is supported



# New Style Rapid Prototyping

## ◆ Need

- Supporting a functionality in special-purpose hardware can save 100 to 1000-fold power/energy over software solutions
  - It is both necessary and possible to model large parts of complex systems involving special purpose hardware to determine feasibility, performance and design tradeoffs
- ## ◆ Prototyping does not increase time to market if done using modern tools
- Resuable IP, Modularly refineable designs
  - Realistic workloads
  - Should lead from FPGAs to ASICs directly



# An unsolved problem

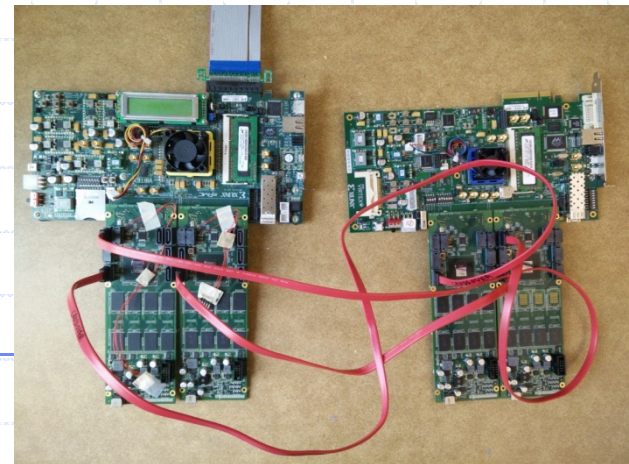
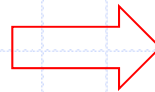
- ◆ Even if the design cost can be reduced dramatically, the NRE of a new chip requires a huge market to amortize the upfront expense
- ◆ May be 3D stacking will provide a way
- ◆ May be a new type of reconfigurable architecture substrate will bring the FPGA closer to ASICs in power efficiency
  - see James Hoe's work



# The future

- ◆ Architecture research community has to dramatically expand its scope
  - not just microarchitectures but all the software issues related to HW-SW codesign
- ◆ Systems are getting too complex to be designed in an *ad hoc* manner
  - Need for more formal methods and tools
- ◆ End of Moore's law will probably create more jobs for architects
  - Special-purpose hardware may be the best solution for *dark silicon*

# Simulation is Passé; all Future Systems Require FPGA Prototyping



Thanks